Xiaokun Yang, Ph.D.
Assistant Professor
University of Houston Clear Lake

Contact Info

Address: 2700 Bay Area Blvd, Houston, Texas 77058
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Personal Web: http://sceweb.uhcl.edu/xiaokun
OpenIC: https://sceweb.sce.uhcl.edu/xiaokun/OpenIC/
Google Scholar: https://scholar.google.com/citations?hl=en&user=GQw5udEAAAAJ

Research Interests

- ASIC/FPGA Acceleration on AI/ML
- System-on-Chip (SoC) Architecture on IoT/Edge Devices
- HW/SW Co-Design and Verification Methodology on ASIC/FPGA/SoC

Education

Florida International University, Miami, FL 2016
Ph.D., Computer Engineering
- Dissertation: *A High Performance AES-Encrypted On-Chip Bus Architecture for Internet-of-Things (IoT) System-on-Chips (SoC)*
- Advisor: Jean H. Andrian, Ph.D

Florida International University, Miami, FL 2007
M.S., Computer Engineering
- Thesis: *USB 2.0 Host Controller Design and Verification*
- Advisor: Jean H. Andrian, Ph.D

Beihang University, Beijing, China 2008
M.S., Software Engineering
- Advisor: Jinming Dong, Ph.D

Beihua University, Jilin, China 2005
B.S., Electrical and Computer Engineering

Work Experience

Assistant Professor 2016 – Present
Computer Engineering
University of Houston Clear Lake **(UHCL)**

Sr. ASIC Design/Layout Engineer 2011 – 2012
GPU, Advanced Micro Devices **(AMD)**
Chip tape-out experiences : AMD CPUs/GPUs/APUs – Kabini, Kaveri, Bonaire, Kryptos, and Samara

Sr. ASIC Verification Engineer 2009 – 2010
WLAN, China Electronics Corp. (CEC)
Chip tape-out experiences : 802.11 a/b/g/n MIMO Mixed-Signal SoCs – CEC TL3 and TL5

ASIC Design Engineer 2007 – 2008
SoC Group, PowerLayer MicroSystems Corp. (PLM)
Chip tape-out experiences : PLM High-Definition TV (HDTV) SoCs – PLM3K and PLM5K

Honors, Awards, and Certificates

Research Grant:

- Co-PI: NSF MRI #2019018, Pending 2020
- PI: Xilinx University Program #5310-XUP-1-19PQJCF, Awarded 2020
- PI: NSF CAREER #1846315, Not Awarded 2018
- PI: NSF Travel Grant, Demo Session on SEC2017, Awarded 2017
- PI: NSF Travel Grant, Workshop on ICAC2017, Awarded 2017
- PI: Cisco Research & Open Innovation, Not Awarded 2017
- PI: Faculty Research and Support Funds (FRSF), Awarded, UHCL 2019 – 2020
- PI: Faculty Research and Support Funds (FRSF), Awarded, UHCL 2018 – 2019
- PI: Faculty Research and Support Funds (FRSF), Awarded, UHCL 2017 – 2018
- PI: Faculty Development Funds (FDF - ISQED 2019, CSCI 2018, ICACS 2018, SEC 2017, ICAC 2017, ASAP 2017), Awarded, UHCL
- PI: Anthony & Barbara Lekkos Endowment, Not Awarded, UHCL 2018
- PI: GRA, Not Awarded, UHCL 2017
- PI: Faculty Fellowship, Not Awarded, UHCL 2017

Awards:

- New Faculty Research Award Nomination, UHCL 2020
- Piper Teaching Award Nomination, UHCL 2018
- Best Poster Award, DataCom, Orlando, FL 2017
- Best Ph.D Forum Paper Award, ISVLSI, Tampa, FL 2014
- Dissertation Year Fellowship, FIU 2015 – 2016
- Teaching/Research Assistant Scholarship, FIU 2012 – 2015
- Graduate Student Appreciation Week (GSAW) Scholarship, FIU 2016
- SGA Graduate Scholarship, FIU 2015
- Graduate Student Travel Grant (GPSC), DAC2016, FIU 2016
- Graduate Student Travel Grant (GPSC), ISVLSI2014, FIU 2014
- Graduate Student Travel Grant (GPSC), SSST2013, FIU 2013
- Presidential Fellowship Nomination, FIU 2012
- Student Chair, Social Planning Dept., FIU China Alumni Association 2009 – Present
- Outstanding Graduate Representative (2/120), Beihang University 2007
- Outstanding Student Leader (14/500), Beihang University 2006 – 2007
- Student President (1/65) of Beihang–FIU Engineering Program 2005 – 2007

Industrial Certificates & Training:

- UVM Methodology Training, **AMD** 2012
- IP/SoC Tree Working Environment Training, **AMD** 2012
- dj/dv/perl/C++ Verification Environment Training, **AMD** 2012
- System Verilog and UVM Training, **Mentor Graphic** 2011
- Low-Power Technology Training (CPF design flow), **Cadence** 2011
- Assertion Training, **Synopsys** 2011
- ARM Technical Training Course, 12th to 13th October, **ARM** 2010
- Mixed-Signal Technologies – AMS tool introduction, **Cadence** 2010
- Constraint-Random Test and Coverage Training, **Synopsys** 2009
- VMM Verification Methodology, **Synopsys** 2009
- DesignWare IP Integration Training (USB2.0 OTG Controller, Ethernet Controller),

Synopsys 2008

- DC and Layout Training, **Mentor Graphic** 2007
- Integrated Circuit Design Flow Training, **Mentor Graphic** 2006
- EDA Tools Training, ModelSim and VIM, **Mentor Graphic** 2005

Publications (2013–Present)

Patents:

1. **X. Yang** and J. Andrian, "An Advanced Bus Architecture for AES-Encrypted High-Performance Embedded Systems," US Patent, **US20170302438A1**, Oct. 19, 2017.
2. **X. Yang**. 2013."A Mixed-Signal Verification System for Sigma-Delta Filters," **CN102955871A**.
3. W. Teng, J. Sun, L. Mo, J. Zou, Y. Wu, F. Liao, and J. Zhang, **X. Yang**, Ding Li. 2013. "ethod and device for detecting frame signals of wireless local area network (WLAN) equipment," **CN102970688A**.

Journals:

1. [**J SUPERCOMPUT 2021**] I. Westby and **X. Yang**, "Exploring FPGA Acceleration on a Multi-Layer Perceptron Neural Network for Digit Recognition," The Journal of Supercomputing *(***J SUPERCOMPUT - IF: 2.469)**, Submitted, 2020.
2. [**M SYST 2021**] X. Zhang, X. Fu, J. Lu, **X. Yang**, I. Unwala, "Face Recognition using Deep k-Nearest Neighbors in Intelligent Safety and Security Monitoring System," Multimedia Systems, *(***J SUPERCOMPUT - IF: 1.734)**, Submitted, 2020.
3. [**ToE 2020**] **X. Yang**, "Bridging the Gap Between Academia and Industry Needs with An Open Source Platform in Teaching Digital System Design," IEEE Trans. on Education *(***ToE - IF: 2.274)**, Second Round Review, April 2020.
4. [**NNW 2020**] H. He, L. Wu, and **X. Yang** "Iterated Dilated Convolutional Neural Networks for Word Segmentation," Neural Network World *(***NNW - IF: 0.957)**, Second Round Review, 2020.
5. [**IET-CDT 2020**] **X. Yang**, S. Sha, I. Unwala, and J. Lu, "Towards Third-Part IP Integration: A Case Study of High-Throughput and Low-Cost Wrapper Design on A Novel IBUS Protocol," IET Computers & Digital Techniques *(***IET-CDT - IF: 0.857)**, Accepted, 2020.
6. [**JCSC 2019**] **X. Yang** and S. Shi, "Exploiting Energy-Quality (E-Q) Tradeoffs on Approximate FPGA Designs of Scalable Sequential Circuits," Journal of Circuits, Systems and Computers *(***JCSC - IF: 0.595)**, Accepted, 2019.
7. [**TODAES 2019**] S. Sha, A. S. Bankar, **X. Yang**, W. Wen, and G. Quan, "On Fundamental Principles for Thermal-Aware Design on Periodic Real-Time Multi-Core Systems," ACM Trans. on Design Automation of Electronic Systems *(***TODAES - IF: 0.924)**, Accepted, 2019.
8. [**JoC 2019**] **X. Yang**, et. al., "A Vision of Fog Systems with Integrating FPGAs and BLE Mesh Network," Journal of Communications (JoC), Vol. 14, No. 3, PP. 210-215, March 2019.

9. [**JETC 2018**] **X. Yang**, W. Wen, and M. Fan, "Improving AES Core Performance via An Advanced IBUS Protocol," ACM Journal on Emerging Technologies in Computing **(JETC - IF: 2.055)**, Vol. 14, No. 1, PP. 61-63 , Jan. 2018.

10. [**IJCA 2018**] Y. Zhang, **X. Yang**, etc., "Hierarchical Synthesis of Approximate Multiplier Design for Field-Programmable Gate Arrays (FPGA)-CSRmesh System," Intl. Journal of Compt. Applications (IJCA), Vol. 180, No. 17 PP. 1-7, Feb. 2018

11. [**VLSID 2017**] **X. Yang**, N. Wu, and J. Andrian, "Comparative Power Analysis of An Adaptive Bus Encoding Method on The MBUS Structure," Journal of VLSI Design *(***VLSID)**, Vol. 2017, No. 4914301, PP. 1-7, May 2017.

12. [**JSS 2017**] M. Fan, Q. Han, and **X. Yang**, "Energy Minimization for On-Line Real-Time Scheduling with Reliability Awareness," Elsevier Journal of Systems and Software. *(***JSS - IF: 2.559)**, Vol. 127, PP. 168-176, May 2017.

13. [**IJCA 2017**] J. Thota, P. Vangali, and **X. Yang**, "Prototyping An Autonomous Eye-Controlled System (AECS) Using Raspberry-Pi on Wheelchairs," Intl. Journal of Compt. Applications (IJCA), Vol. 158, Issue 8, PP. 1-7, Jan. 2017.

14. [**CAE 2017**] P. Vangali and **X. Yang**, "A Compression Algorithm Design and Simulation for Processing Large Volumes of Data from Wireless Sensor Networks," Communications on Applied Electronics (CAE), Vol. 7, Issue 4, PP. 1-5, June 2017.

15. [**Integration 2016**] **X. Yang**, N. Wu, and J. Andrian, "A Novel Bus Transfer Mode: Block Transfer and A Performance Evaluation Methodology," *(***Elsevier, Integration, the VLSI Journal - IF: 1.15)**, Vol. 52, Issue: C, PP. 23-33, Jan. 2016.

16. [**IJDKP 2016**] K. Zeng, N. Wu, **X. Yang**, and K. K. Yen, "FHCC: A Soft Hierarchical Clustering Approach For Collaborative Filtering Recommendation," Intl. Journal of Data Mining & Knowledge Management Process (IJDKP), Vol.6, No.3, May 2016.

17. [**TVLSI 2015**] **X. Yang** and J. Andrian, "A High Performance On-Chip Bus (MSBUS) Design and Verification," IEEE Trans. Very Large Scale Integr. (VLSI) Syst. *(***TVLSI - IF: 1.946**), Vol. 23, Issue: 7, PP. 1350-1354, July 2015.

Conferences:

1. [**ICAI 2020**] I. Westby, H. Koc, J. Lu, and **X. Yang**, "A Design on Multilayer Perceptron (MLP) Neural Network for Digit Recognition," The 22nd Intl. Conf on Artificial Intelligence (ICAI 2020), Accepted, March 2020.

2. [**ICAI 2020**] **X. Yang**, T. Andrew Yang, and L. Wu, "An Edge Detection IP of Low-cost System-on-Chip for Autonomous Vehicles," The 22nd Intl. Conf on Artificial Intelligence (ICAI 2020), Accepted, March 2020.

3. [**ICAI 2020**] A. Gajjar, S. Dave, T. Andrew Yang, L. Wu, and **X. Yang**, "An IoT-Edge-Server System with BLE Mesh Network, LBPH, and Deep Metric Learning," The 22nd Intl. Conf on Artificial Intelligence (ICAI 2020), Accepted, March 2020.

4. [**CSCE 2020**] L. Wu, A. Yang, A. Dubrovskiy, H. He, H. Yan, **X. Yang**, et. al, "Advancing AI-aided Computational Thinking in STEAM (Science, Technology, Engineering, Arts, Math) Education (Act-STEAM)," The 2020 World Congress in Computer Science, Computer Engineering, and Applied Computing (CSCE), 2020.

5. [**CSCE 2020**] L. Wu, A. Yang, H. Yan, **X. Yang**, et. al, "Realistic Drawing & Painting with AI Supported Geometrical and Computational Method (Fun-Joy)," The 2020 World Congress in Computer Science, Computer Engineering, and Applied Computing (CSCE), 2020.

6. [**ISQED 2019**] **X. Yang**, Y. Zhang, and L. Wu,"A Scalable Image/Video Processing Platform with Open Source Design and Verification Environment," 20th Intl. Symposium on Quality Electronic Design *(***ISQED 2019)**, PP. 110-116, Santa Clara, CA, USA, 2019.

7. [**ISVLSI 2019**] Vaca, K., A. Gajjar, and **X. Yang**, "Real-Time Automatic Music Transcription (AMT) with Zync FPGA," 2019 IEEE Computer Society Annual Symposium on VLSI *(***ISVLSI 2019, Acceptance Rate: 17%)**, PP. 378-384, Miami, FL, USA, 2019.

8. [**ISVLSI 2019**] Zhang Y., **X. Yang**, "A Case Study On Approximate FPGA Design With an Open-Source Image Processing Platform" 2019 IEEE Computer Society Annual Symposium on VLSI *(***ISVLSI 2019, Acceptance Rate: 17%)**, PP.372-377, Miami, FL, US, 2019.

9. [**ISMCR 2019**] K. Vaca, M. Jefferies, and X. Yang , "An Open Real-Time Audio Processing Platform on Zync FPGA," Intl. Symposium on Measurement and Control in Robotics (ISMCR 2019), PP. D1-2-1-D1-2-6, Houston, TX, USA, 2019.

10. [**ISMCR 2019**] X. Zhang, J. Lu, X. Fu, **X. Yang**, I. Unwala, and T. Zhang, "Tracking of Targets in Mobile Robots Based on Camshift algorithm," Intl. Symposium on Measurement and Control in Robotics (ISMCR 2019), PP. B2-3-1-B2-3-5., UHCL, Houston, USA, Sept 19-21, 2019.

11. [**ICAI 2019**] H. He, L. Wu, H. Yan, and **X. Yang**, "Synthesize Corpus for Chinese Word Segmentation," The 21st Intl. Conference on Artificial Intelligence (ICAI 2019), PP.129-134, Las Vegas, NV, USA, 2019.

12. [**HONET-ICT 2019**] J. Gopaluni, I. Unwala, J. Lu, and **X. Yang**, "Graphical User Interface for OpenThread," 2019 IEEE 16th Intl. Conference on Smart Cities: Improving Quality of Life Using ICT & IoT and AI (HONET-ICT 2019), PP. 235-237, Charlotte NC, USA, Oct. 6-9, 2019.

13. [**CSE 2019**] X. Fu, J. Lu, X. Zhang, **X. Yang**, and I. Unwala, "Intelligent in-vehicle safety and security monitoring system with face recognition," 2019 IEEE Intl. Conference on Computational Science and Engineering (CSE 2019), PP. 225-229, New York, NY, USA, Dec. 05 2019, 2019.

14. [**CSCI 2018**] A. Gajjar, **X. Yang**, et.al., "Mesh-IoT Based System For Large-Scale Environment," 5th Annual Conf. on Computational Science & Computational Intelligence (CSCI 2018), PP. 1019-1023, Las Vegas, NV, USA, 2018.

15. [**CSCI 2018**] J. Gopaluni, I. Unwala, J. Lu, and X. Yang , "Implementation of GUI for OpenThread," 5th Annual Conf. on Computational Science & Computational Intelligence (CSCI 2018), PP. 1015-1018, Las Vegas, NV, USA, 2018.

16. [**ICACS 2018**] A. Gajjar, **X. Yang**, et. al.., "An FPGA Synthesis of Face Detection Algorithm using HAAR Classifiers," Intl. Conference on Algorithms, Computing and Systems (ICACS 2018), PP.133-137, July 27-29, Beijing China, 2018.

17. [**ICACS 2018**] Y. Zhang, **X. Yang**, et. al., "Exploring Slice-Energy Saving on An Video Processing FPGA Platform with Approximate Computing" Intl. Conference on Algorithms, Compting and Systems (ICACS 2018), PP.138-143, July 27-29, Beijing China, 2018.

18. [**ITNG 2018**] H. He, L. Wu, **X. Yang**, et. al., "Dual Long Short-Term Memory Networks for Sub-Character Representation Learning," The 15th Intl. Conference on Information Technology - New Generations (ITNG 2018), Springer Advances in Intelligent Systems & Computing Book Series, Springer-Verlag, Las Vegas, NV, USA, 2018.

19. [**DASC 2017**] L. Nwosu, H. Wang, J. Lu, I. Unwala, **X. Yang**, et. al., 'Deep Convolutional Neural Network for Facial Expression Recognition Using Facial Parts," 2017 IEEE 15th Intl Conf on Dependable, Autonomic and Secure Computing (DASC 2017, Best Poster Award), PP. 1318-1321, Orlando, FL, USA, 2017.

20. [**ASP-DAC 2017**] **X. Yang** and W. Wen, "Design of A Pre-Scheduled Data Bus (DBUS) for Advanced Encryption Standard (AES) Encrypted System-on-Chips (SoCs)," The 22nd Asia and South Pacific Design Automation Conference, **(ASP-DAC 2017 - Regular Paper, Acceptance Rate:111/358=31%)**, PP. 506-511, Chiba, Japan, Jan. 2017.

21. [**SEC 2017**] **X. Yang** and X. He, "Establishing a BLE Mesh Network using Fabricated CSRmesh Devices," The 2nd ACM/IEEE Symposium on Edge Computing **(SEC 2017)**, No. 34, San Jose/Fremont, CA, US, 2017.

22. [**AHFE 2017**] **X. Yang** and N. Wu, "Design of A Bio-Feedback Digital System (BFS) Using 33-Step Training Table for Cardio Equipment," The 8th Intl. Conference on Applied Human Factors and Ergonomics (AHFE 2017), PP. 53-64, Los Angeles, California, 2017.

23. [**ICAC 2017**] **X. Yang**, Y. Zhang, W. Wen, and M. Fan, "A Case Study of Self-Organization Algorithms for High-Efficiency System-on-Chips Integration," IEEE Intl. Conf. on Autonomic Computing (ICAC 2017) – Workshop on Feedback Computing, Columbus, Ohio, US, 2017.

24. [**FYEE 2017**] N. Wu, K. Zeng, J. Weidenfeller, and **X. Yang**, "Flipping the Classroom for Enhancing Learning and Designing in an Embedded Systems Class, " The 1st Year Engineering Experience Conference (FYEE 2017) , PP.1-4, Daytona Beach, FL, 2017.

25. [**ICI 2017**] D. Wu, N. Wu, K. Zeng, and **X. Yang**, "Recognizing Unconstrained Handwritten Digit Based on Shape Analysis and Multi-class SVM Classification," The 8th Intl. Conference on Information (ICI 2017), Tokyo, Japan, May 2017.

26. [**SEC 2017**] A. Gajjar, Y. Zhang, and **X. Yang**, "A Smart Building System Integrated with An Edge Computing Algorithm and IoT Mesh Networks," The Second ACM/IEEE Symposium on Edge Computing **(SEC 2017)**, Article No. 35, San Jose/Fremont, CA, US, 2017.

27. [**DAC 2016**] **X. Yang** and J. Andrian, "A Configurable and Synthesizable On-Chip Bus Architecture for Integrating Industrial Standard IPs," 2016 Design Automation Conference *(***DAC 2016)**, WIP, Austin, TX, USA, June 2016.

28. [**ISVLSI 2014**] **X. Yang** and J. Andrian, "A Low-Cost and High-Performance Embedded System Architecture and An Evaluation Methodology," IEEE Computer Society Annual

Symposium on VLSI *(***ISVLSI 2014 - Best Ph.D Forum Paper Award)**, PP. 240-243, Tampa, FL, USA, 2014.

29. [**SSST 2013**] **X. Yang** X. Niu, and J. Fan, "Mixed-Signal System-on-Chip (SoC) Verification Based on System Verilog Model," The 45th Southeastern Symposium on System Theory (SSST 2013), PP. 17-21, Waco, TX, USA, 2013.

Abstracts:

1. [**Dual 2019**] Isaac Westby and **X. Yang**, "Real-time Digit Recognition with Neural Network on a Video Processing FPGA Platform," 2018 IEEE Innovation and Automation Conference, Gilruth Recreation Center, NASA-JSA, Houston, Nov. 15, 2019.
2. [**ICAMSE 2019**] **X. Yang**, "An Advanced SoC Architecture for Low-Cost And Low-Power Edge Devices," International Conference on Advanced Materials Sciences and Engineering, Osaka, Japan, 2019
3. [**Robotics 2018**] **X. Yang**, Y. Zhang, A. Gajjar, H. Schmoyer, and N. Ly, "Learning-on-Chip: Facial Detection with Approximations of FPGA Computing," 2018 Robotics & AI Day, UHCL, Aug. 03, 2018.
4. [**Dual 2018**] **X. Yang**, "A Scalable Image/Video Processing Platform with FPGA Design and Verification Environment," 2018 IEEE Innovation and Automation Conference, Gilruth Recreation Center, NASA-JSA, Houston, Nov. 3, 2018.
5. [**Dual 2018**] A. Gajjar, **X. Yang**, "Mesh-IoT Based Smart and Secure System for Wide-Range Territory," 2018 IEEE Innovation and Automation Conference, Gilruth Recreation Center, NASA-JSA, Houston, Nov. 3, 2018.
6. [**Dual 2017**] **X. Yang**, "A Prototype in Fog Computing (FC) : Design of An FPGA-CSRmesh (FC) Platform Toward Wide-Area and Low-Energy IoT Networks, '' 2017 IEEE Innovation and Automation Conference, Gilruth Recreation Center, NASA-JSA, Houston, Oct. 28, 2017.
7. [**Robotics 2017**] Y. Zhang and **X. Yang**, "Exploring Approximate Designs for FPGA-Based Edge Computing," 2017 Robotics & AI Day, UHCL, July 21, 2017.
8. [**Robotics 2017**] A. Gajjar and **X. Yang**, "A Smart Building System Integrated with An Edge Computing Algorithm and IoT Mesh Networks," 2017 Robotics & AI Day, UHCL, July 21, 2017.
9. [**Dual 2017**] Y. Zhang and **X. Yang**, "A Novel Fog Computing Acceleration Method: Approximate FPGA Design on Adder and Multiplier," 2017 IEEE Innovation and Automation Conference, Gilruth Recreation Center, NASA-JSA, Houston, Oct. 28, 2017.
10. [**Dual 2017**] A. Gajjar and **X. Yang**, "A Wide Area IoT Mesh Network With Edge Computing," 2017 IEEE Innovation and Automation Conference, Gilruth Recreation Center, NASA-JSA, Houston, Oct. 28, 2017.
11. [**GBS 2016**] **X. Yang**, "A High Performance Advanced Encryption Standard (AES)-Encrypted On-Chip Bus Architecture for Internet-of-Things (IoT) System-on-Chips (SoCs)," IEEE Galveston Session, NASA-JSA, Gilruth Recreation Center, Nov. 17, 2016.

RESEARCH ACTIVITIES:

Membership:

- IEEE Member 2013–
- IEEE Young Professionals 2014–
- TC on Autonomous Driving Technologies (TCADT) 2020–
- TC on VLSI (TCVLSI) 2020–
- TC on Electronic Design Automation (CEDA) 2020–
- ACM Member 2016–
- SIG in Artificial Intelligence (SIGAI) 2020–
- IACSIT Senior Member 2018–

Editorial Board:

- Journal of Communications (JoC) 2018–
- Journal of Electronics Communication and Computer Engineering (IJECCE) 2018–
- Associate Editor, ICAI Proceedings 2020

Journal/Book Reviewer:

- IEEE Trans. on VLSI Syst. (TVLSI) 2015, 2017, 2019
- IEEE Trans. on Education (ToE) 2019
- IEEE Trans. on Industrial Informatics (TII) 2018
- Integration, the VLSI Journal (VLSI) 2017, 2019
- IET Computer & Digital Techniques (IET-CDT) 2017-1, 2017-2, 2019, 2020
- SN Computer Science 2020
- Sustainable Computing, Informatics and Systems (SUSCOM) 2019
- Book proposal - The Thermal-Constrained Real-Time Scheduling on Multi-Core Platforms-An Analytical Approach 2019
- CRC Press Book: Empowering the High-Performance Computing by Process-in-Memory on 3D Processors 2019

ACM Computing Reviewer (CR):

- IEEE Trans. on Compt. (TC) 2017-1, 2017-2
- ACM Trans. on Design Automation of Electronic Syst. (TDAES) 2016, 2018
- ACM Journal on Emerging Technologies in Computing Systems (JETC) 2015, 2019
- ACM Trans. on Modeling and Computer Simulation 2017
- Integration, the VLSI Journal (VLSI) 2018
- Microprocessors & Microsystems 2016, 2017-1, 2017-2, 2018
- Springer Book: Design Automation Techniques for Approximation Circuits, ISBN 978-3-319-98964-8 2018

International Conference Chair & TPC:

- Associate Editor/Track Chair, Symposium/Workshop - Hardware Acceleration on AI, Intl. Conference on Artificial Intelligence (ICAI 2020), July 2002.
- Publication Chair: 2019 2nd Intl. Conference on Algorithms, Computing and Artificial Intelligence (ACAI 2019), Sanya, China, Dec., 2019, 2020
- Section Chair: Circuit, Reliability and Fault Tolerance II in IEEE Computer Society Annual Symposium on VLSI (ISVLSI 2019), Miami , FL, US, July, 2019.
- Section Chair: Symposium on Internet of Things & Internet of Everything in the 5th Annual Conf. on Computational Science & Computational Intelligence (CSCI2018), Las Vegas, Nevada, USA, Dec., 2018.

- Section Chair: the IoT section of the 2017 IEEE Innovation and Automation Conference, Guilruth ctr., NASA, Oct., 2017.
- TPC: 2nd Intl. Conference on on Microelectronic Devices and Technologies (MicDAT 2020), Tenerife (Canary Islands), Spain, June, 2020.
- TPC: The 3rd International Conference on Computer Systems and Communication Technology (ICCSCT 2020), Guangzhou, China, Aug. 20-21, 2020.
- TPC: 2019 IEEE 16th International Conference on Smart Cities: Improving Quality of Life Using ICT & IoT and AI (HONET-ICT 2019), Charlotte NC, US, Oct., 2019.
- TPC: Intel. Conference on Frontiers of Control and Sensor Networks (CFCSN 2019), Prague, Czech Republic, Nov. 25-27, 2019
- TPC: The 7th Intl. Conference on Computer and Communications Management (ICCCM 2019), Bangkok, Thailand, July 27-29, 2019.
- TPC: IEEE 4th Intl. Conference on Communication and Information Systems (ICCIS 2019), Wuhan, China, Dec. 21-23, 2019
- TPC: Intl. Conference on Computer Science and Software Engineering (CSSE 2019), Xi'an, China, May 24-26, 2019
- TPC: The World Symposium on Software Engineering (WSSE 2019), Wuhan, China, Sept. 20-23, 2019.
- TPC: Intl. Conference on Communications and Future Internet (ICCFI 2019), Bangkok, Thailand, July 27-29, 2019
- TPC: The 2nd Intl. Conference on on Microelectronic Devices and Technologies (MicDAT 2019), Amsterdam, Netherlands, May 15-17, 2019
- TPC: Intl. Workshop on Computer Science and Engineering (WCSE 2019), Hongkong, China, June 15-17, 2019.
- TPC: Intl. Conference on Computing, Networking and Communications (ICNC 2019), Honolulu, Hawaii, USA, Feb. 18-21, 2019
- TPC: IEEE 3rd Intl. Conference on Communication and Information Systems (ICCIS 2018), Singapore, Dec. 28-30, 2018.
- TPC: The 2nd Intl. Conference on Algorithms, Computing, and Systems (ICACS 2018), Beijing, China, July 27-29, 2018
- TPC: The 8th Intl. Workshop on Computer Science and Engineering (WCSE 2018), Bangkok, Thailand, June 28-30, 2018
- TPC: The 1st Intl. Conference on Microelectronic Devices and Technologies (MicDAT 2018), Barcelona, Castelldefels, Spain, June 20-22, 2018.
- TPC: IEEE/ACM Intl. Symposium on Nanoscale Architectures (Nanoarch 2017), Newport, USA, July 25-26, 2017
- TPC: The 3rd Annual International Conference on Electronics, Electrical Engineering and Information Science (EEEIS 2017), Guangzhou, China, Spet. 8-10, 2017
- TPC: The 2nd International Conference on Computer Science and Technology (CST 2017), Guilin, China, May 26-28, 2017
- Reviewer - The 17th Intl. Symposium on Quality Electronic Design (ISQED 2016)
- Reviewer - The 11th IEEE Intl. Conference on Network, Architecture and Storage (IEEE NAS 2016)
- Reviewer - The 49th Proceedings of the 8th International Workshop on Network on Chip Architecture (NocArc 2015)

University/College/Department/Program Services:

- Student Affairs Committee 2017 – 2018

- Advisory Board Meetings 2016–
- New Student Reception FA 2019, SP 2019
- Graduate Preview FA 2019, SP 2019
- UG/G Open House FA 2016-2017-2018, SP 2016-2017-2018
- UG/G Open House FA 2016-2017-2018, SP 2016-2017-2018
- Student Commencement FA 2018
- Houston Robotics & AI Day, Oral Presenter, UHCL 2017
- IEEE Student Branch Professor's Day, UHCL, Oral Presenter 10/2016

Community Services:

- Judge, Science & Engineering Fair of Houston, 2019, 2020
- GSAW Scholarly Forum, Oral Presenter March 2016
- 2015 Miami Maker Faire, IoT Device Exhibitor Feb. 2015
- 2014 Hongkong Electronics Faire (Autumn Edition), IoT Device Exhibitor Spet. 2015
- IEEE Workshop – Industrial Standard Integrated Circuit Design Flow, Invited Talk Aug. 2013

Teaching Experience

Thesis chair – Integrated Circuit & System (ICS) Lab: 2016 – Present

- April Reed (Current thesis students)
  Thesis: Exploiting Area-Speed-Power Tradeoff of FPGA Designs on Multilayer Perceptron (MLP) Neural Network.
- Schmoyer, Harold William (Current thesis students)
  Thesis:Hardware Acceleration for Real-time Image Processing
- Isaac Westby, Thesis Student, Spring 2020
  Thesis: Accelerating Digit Recognition by Neural Network with FPGA
  Publication at ICS Lab: ICAI2020, J SUMPERCOMPT (under review)
  Current status: Graduate Applications Engineer with ARM
- Yunxiang Zhang, Thesis student, Fall 2018
  Thesis: A scalable image/video processing platform with approximate FPGA design
  Publication at ICS Lab: ICACS2018, IJCA2018, ISVLSI2019, FC2017, SEC2017, ISQED2019
  Current status: Ph.D Candidate
- Archit Gajjar, Thesis student, Spring 2019
  Thesis: A smart building system integrated with BLEMesh and synology server
  Publication at ICS Lab: SEC2017, ICACS2018, CSCI2018, JC, IJCA, ISVLSI2019
  Current status: Ph.D Candidate

Thesis Committee: 2016 – Present

- Xin Zhang (Current thesis student)
  Thesis: Tracking System for the Drone with Zynq Platform
- Xiaodi Fu, Fall 2019
  Thesis: Intelligent In-vehicle Safety and Security Monitoring System
- Vamsi Krishna Karanam, Fall 2019
  Thesis: Cyber Physical / Embedded Systems
- Hui Wang, Fall 2018
  Thesis: ECamera: A Real-time Facial Expression Recognition System

- Jitendra Gopaluni, Fall 2018
  Thesis: Implementation of a Graphical User Interface for Thread Protocol using OpenThread Platform
- Han He, Spring 2018
  Thesis: Industrial Strength Dependency Parsing System
- Lucy Nwosu, Fall 2017
  Thesis: A Hybrid Feature Extraction Algorithm for Facial Expression Recognition Using Convolutional Neural Network.

Research project – Integrated Circuit & System (ICS) Lab: 2016 – Present

- Vasundhara Kakda, Hetal Dilip Rathod (Current graduate students)
  Research Project: Hardware Acceleration on Edge Detection for Autonomous Vehicles
- Naveen Kumar Chennoju, Dilip Aravind Kari, Venkata Kaustubha Ayaluri (Current graduate students)
  Research Project: Smart Parking System with Nexys FPGA
- Kevin Vaca, Undergraduate student, Fall 2019
  Research Project: Real-Time Automatic Music Transcription (AMT) with Zync FPGA
  Publication at ICS Lab: ISVLSI2019
- Priyanka Vangali, graduate student, Fall 2017
  Research Project: A Compression Algorithm Design and Simulation for Processing Large Volumes of Data from Wireless Sensor Networks
  Publication at ICS Lab: CAE 2017
- Jayanth Thota, graduate student, Fall 2017
  Research Project: Prototyping An Autonomous Eye-Controlled System (AECS) Using Raspberry-Pi on Wheelchairs
  Publication at ICS Lab: IJCA 2017

Teaching – UHCL: 2016 – Present

- Advanced Digital System Design (CENG5534)
- Digital System Design (CENG4354)
- Senior Project I&II (CENG4265&CENG4266)
- Electronics (CENG3316)
- Lab for Electronics (CENG3116)
- Lab for Linear Circuit (CENG2113)
- Lab for Digital Circuit (CENG2112)

Primary Lab Instructor/TA – FIU: 2012 – 2015

- Circuit Lab (EEL3110: Fall 2012)
- Electronic I Lab (EEL3303: Spring 2013, Summer 2013, Fall 2013)
- Electronic II Lab (EEL4303: Spring 2014, Summer 2014, Spring 2015, Summer 2015)

Specialized Skills

Methodologies, Languages, and EDA Tools:

- Professional in industry ASIC/FPGA/SoC design flow
- Professional in hardware description language: Verilog and VHDL
- Professional in hardware verification language: System Verilog

- Professional in design flow scripts: dj, dv, tcl, cshell, Makefile, perl
- Professional in verification methods: ADV, CDV, CRV
- Professional in UNIX/LINUX and EDA tools: Vim; Debussy/Verdi; ModelSim/Questa, NC, VCS, Quasta; DC, PT and so on.
- Professional in FPGA tools: Xilinx ISE/Vivado, Intel Quartus
- Professional in verification methodology – VMM and UVM
- Professional in low power design methods: clock gate and power domain design methods (CPF and UPF)
- Familiar with mix-signal verification methods: SPICE, AMS, RVM

Industrial Specifications:

- Professional in SoC architectures: AMBA APB, AHB, AXI, OCP, Wishbone.
- Professional in SoC controllers: ARM/MIPS, DMA, DDR2 Controller.
- Professional in security protocols: AES and DES.
- Professional in interface specifications: USB2.0 OTG – Nano-PHY, VIP, UTMI+; IEEE 802.3x Ethernet – MII/RMII Phy; PCIE; Infrared Remote.
- Professional in Wireless communication Protocols: Wi-Fi 802.11a/b/g/n Baseband, Bluetooth 4.0 (LE).
- Professional in SoC peripherals: Interrupt Controller, Semaphore, UART, I2C, SPI, SDIO, GPIO, WatchDog, Timer, and so on.
- Professional in memory controllers: Smart Card, NAND/NOR/Serial Flash, E2ROM.
- Familiar with graphic modules: TNR, SNR, SCALER, SE, Pre-Processing, Post-Processing.
- Familiar with mix-signal model design: DA, DeMux, Delta Sigma Modulator, LNA, Mixer, VGA, AD, PA, and DA.