COURSE SYLLABUS

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YEAR COURSE OFFERED: 2019

SEMESTER COURSE OFFERED: Spring

DEPARTMENT: CENG

COURSE NUMBER: 3312

NAME OF COURSE: Digital Circuits

NAME OF INSTRUCTOR: Vernon Bryant

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The information contained in this class syllabus is subject to change without notice. Students are expected to be aware of any additional course policies presented by the instructor during the course.

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Pre-requisites

Calculus II and Physics II

Learning Objectives

Students will convert numbers from/to Decimal to/from Binary and other Radix systems.
Students will derive equivalent switching expressions by applying transformations allowed in Boolean Algebra.
Students will determine the sum of minterms and product of maxterms that are equivalent to a given expression.
Students will design and analyze combinational circuits comprised of logic gates, multiplexers and decoders with both single and multiple outputs.
Students will obtain a minimal sum of products of a given switching function by using K-maps.
Students will design a multi-level gate network using gates from a specified set, and/or using XOR gates, and/or using multiplexers
Students will determine the state diagram and the minimized state table for a given sequential system.
Students will design and analyze sequential networks comprised of SR flip-flops, and/or T flip-flops, and/or JK flip-flops and/or D flip-flops and logic gates.

Major Assignments/Exams

(Short exams and homework (unannounced)	10%
Exam I	30%
Exam II	30%
Final (comprehensive)	30%

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Required Reading

Roth, Charles. Fundamentals of Logic Design Seventh Edition. St. Paul: West, 2013.

Recommended Reading

None

List of discussion/lecture topics

Boolean algebra, minterms, maxterms DeMorgan's theorem
NAND, NOR, NOT , AND and OR gates
Karnaugh Maps
Quine- McClusky method
VHDL
Combinational circuit design using SSI and MSI/LSI
Combinational circuit analysis
Programmable Logic Devices
Latches and Flip Flops
Counter design and analysis
Mealy and Moore finite state machines
Synchronous sequential circuit design
Synchronous sequential circuit analysis